



**GALGOTIAS COLLEGE OF ENGINEERING AND TECHNOLOGY**  
1, Knowledge Park-II, Greater Noida, Uttar Pradesh, 201310

**FACULTY PROFILE**

<b>Name of Faculty</b>	Dr. Hemanshi Chugh			
<b>Designation</b>	Assistant Professor -II			
<b>College and Department</b>	GCET, ECE			
<b>Google Scholar ID</b>	<a href="https://scholar.google.com/citations?user=3IPBlgEAAAAJ&amp;hl=en&amp;oi=sra">https://scholar.google.com/citations?user=3IPBlgEAAAAJ&amp;hl=en&amp;oi=sra</a>			
<b>Qualification</b>	<b>UG:</b> B.Tech (ECE)	<b>PG:</b> M.Tech (VLSI Design)		
<b>Ph.D.</b>	<b>Specialization:</b> Low Power VLSI Design <b>Title:</b> Design and Performance Optimization of Nano Scale Vedic Multiplier Architecture			
<b>Experience in Years</b>	<b>Teaching:</b> 4	<b>Industry:</b> -	<b>Research:</b> 4	
<b>No. of Papers Published in Journals</b>	<b>National:</b> -		<b>International:</b> 8	
<b>No. of Paper Published in Conferences</b>	<b>National:</b> 1		<b>International:</b> 3	
<b>No. of Books/ Books Chapters</b>	<b>Books published:</b>	<b>Books edited:</b>	<b>Book chapters published:</b> 1	
<b>No. of Patents</b>	<b>Published:</b>		<b>Granted:</b> 1	
<b>Number of Ph.D./ PG/ UG Guided</b>	<b>Ph.D.:</b> -	<b>PG:</b>	<b>UG:</b>	
<b>Details of Professional Membership</b>				
<b>Details of Achievements/Awards</b>	Commendable Research Award (DTU)			
<b>Details of Grants fetched</b>				
<b>No. of STTPs/ FDPs attended as Resource Person</b>				
<b>No. of Conferences/ Seminars/ STCs/ STTPs/ FDPs attended</b>	<b>Conferences:</b>	<b>Seminar:</b>	<b>STCs/ STTPs/ FDPs:</b> 4	
<b>No. of SWAYAM/ MOOCs attended with certification</b>				