Roll No. : .....

Galgotias College of Engineering and Technology, Greater Noida

Pre University Test (PUT) : Odd / Even Semester 2024 - 2025

Course/Branch	**: B. Tech., ECE**	**Semester**	**: VII**
Subject Name	**: VLSI Design**	**Max. Marks**	**: 100**
Subject Code	**: KEC072**	**Time**	**: 180 min**

CO-1: *Actualize the fundamental principles of VLSI design flow for CMOS circuit design and layout.*
CO-2: *Perform the timing analysis of VLSI circuit using delay models and optimization techniques.*
CO-3: *Design dynamic logic circuits and semiconductor memory architecture.*
CO-4: *Compute the power consumption of a VLSI chip and various techniques of low power design.*
CO-5: *Test the VLSI circuits using different techniques.*

Section – A # 20 Marks (Short Answer Type Questions)

Attempt **ALL** the questions. Each Question is of 2 marks (10 x 2 = 20 marks)

Q. No.		COx	Question Description # Attempt **ALL** the questions. Each Question is of 2 marks
1	a	CO1	Discuss the parameters affecting the threshold voltage. (K2).
	b	CO1	What is channel length modulation? (K1).
	c	CO2	What are the different types of power dissipation? (K1).
	d	CO2	Describe the different components of load capacitance. (K2).
	e	CO3	Discuss the problems in single phase clocking scheme. (K2).
	f	CO3	Differentiate between static power and dynamic power. (K4).
	g	CO4	Explain the domino CMOS logic. (K2).
	h	CO4	Why CMOS transmission gates are preferred over other gates? (K4).
	i	CO5	Explain the term controllability. (K2).
	j	CO5	Define the terms- Defects, Errors. (K1).

Section – B # 30 Marks (Long / Medium Answer Type Questions)

Attempt **ALL** the questions. Each Question is of 6 marks (5 x 6 = 30 marks)

Q.2 (CO-1) : What are the three effects that occur due to the presence of oxygen as impurity in silicon? (K1)

OR

Discuss different types of packaging technologies available for packaging ICs ? (K2)

Q.3 (CO-2) : How interconnect capacitance is estimated? (K3)

OR

Explain Elmore Delay model. Estimate the Elmore delay for a unit inverter driving *m* identical unit inverters. (K2)

Q.4 (CO-3) : Explain the principle of NAND gate flash memory. (K2)

OR

Analyze the problems in single phase clocking circuits (K4)

Q.5 (CO-4) : Explain the basic principles of pass transistor circuits. How are they used in dynamic logic designs? (K2)

OR

Compare SRAM and DRAM in terms of speed, power, and area requirements. (K4)

Q.6 (CO-5) : Describe the design for testability (DFT). (K2)

OR

Section – C # 50 Marks (Medium / Long Answer Type Questions)

Attempt **ALL** the questions. Each Question is of 10 marks.

Q.7 (CO-1) : Attempt any ONE question. Each question is of 10 marks.

a. Describe the three main components of the load capacitance C_{load}, when a logic gate is driving other fan-out gates. (K2)

b. Implements the CMOS logic for the Boolean expression $Y = (A + B)(C + D)$. (K3)

Q.8 (CO-2) : Attempt any ONE question. Each question is of 10 marks.

a. Derive the RC delay model for a CMOS inverter and explain its significance in circuit design. (K4)

b. Discuss the different types of power dissipation in CMOS circuits. Explain techniques to reduce dynamic and static power consumption. (K3)

Q.9 (CO-3) : Attempt any ONE question. Each question is of 10 marks.

a. Explain the concept of energy-delay optimization in VLSI design. How does it impact the overall performance of circuits? (K2)

b. Discuss interconnect modeling and its impact on circuit performance. Explain how Logical Effort can be extended to account for interconnects. (K2)

Q.10 (CO-4) : Attempt any ONE question. Each question is of 10 marks.

a. Explain the read/write operation of SRAM memory cell. How 1-bit cell is used in bigger memory systems? (K2)

b. Describe the working of dynamic CMOS logic circuits. Compare it with static CMOS logic in terms of performance and power consumption. (K4)

Q.11 (CO-5) : Attempt any ONE question. Each question is of 10 marks.

a. Explain in detail the techniques for reducing power consumption in CMOS circuits through voltage scaling and adiabatic logic. (K2)

b. Discuss the Ad Hoc Testable Design Techniques in VLSI systems. How do they enhance fault detection, and what are the trade-offs involved in their implementation? (K3)